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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,210	08/20/2003	Jude A. Rivers	YOR920030249US1	5458

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LAW OFFICE OF CHARLES W. PETERSON, JR. Yorktown
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Herndon, VA 20170

EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2189	

MAIL DATE	DELIVERY MODE
08/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/644,210	RIVERS, JUDE A.	
	Examiner	Art Unit	
	Reba I. Elmore	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2007 and 16 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8, 10-15, 18-23 and 25-29* is/are rejected.

7)☒ Claim(s) *7, 9, 16-17 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/12/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 are presented for examination.

SPECIFICATION

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 103

3. The following is a quotation of 35 USC 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 8, 10-15, 18-23 and 25-29 is rejected under 35 USC 103(a) as being unpatentable over Csoppenszky (P/N 5,802,568) in view of Chai et al. (US 2002/0159283).

5. Csoppenszky teaches the present invention (claims 1 and 19) as claimed including a cache memory and method of managing data in a cache with the cache memory and method comprising:

a cache buffer containing most recently accessed data as a LRU control circuit which also acts as a buffer memory which also tracks the most recently used entries (e.g., see Figure 1 as shown below with support at col. 4, lines 51-61);

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a storage array comprising a plurality of cache memory locations and selectively receiving data from the cache buffer, selectively received the data being stored in memory locations as the an instruction cache (e.g., see col. 1, lines 13-28);

a tag memory storing tags associated with data in the storage array and selected data in the cache buffer as the TLB shown in Figure 1;

providing incoming data to an input buffer as an input register (e.g., see Figure 1, element 160);

selectively loading data from the input buffer into a storage array as the input register having inputs to the CAM which is used to store virtual addresses, a read/write control circuit and a RAM for physical addresses (e.g., see Figure 1, elements 110, 120 and 130 respectively);

selectively loading accessed data from the storage array to an output buffer with a number of most recently accessed data blocks being held in the output buffer as the output buffer being an output circuit which has inputs from elements which contain most recently accessed data blocks thereby making the output buffer capable of storing or holding most recently accessed data blocks (e.g., see Figure 1, element 140); and,

selectively providing data from each of the input buffer, the storage array and the output buffer responsive to an access request as all access requests are selectively provided dependent upon the data requested by the processor or other active elements in the computer system (e.g., see col. 1, lines 8-28).

The reference teaches details of a translation lookaside buffer (TLB) for an instruction cache in a computer system, however, the reference does not use the specifically talk in terms of a cache buffer which contains most recently accessed data or input and output buffers. The

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reference does teach the invention in terms of a TLB which has separate input elements and output elements. The reference also does not use language which specifically discusses selectively receiving and outputting data, however, all cache operate based on the selection of specific instructions and specific data. It would have been obvious to one of ordinary skill in the art at the time the invention was made for the input and output circuitry to be buffers as buffers as among the most commonly used memory devices and are extremely old in the memory art including the memory art using caches.

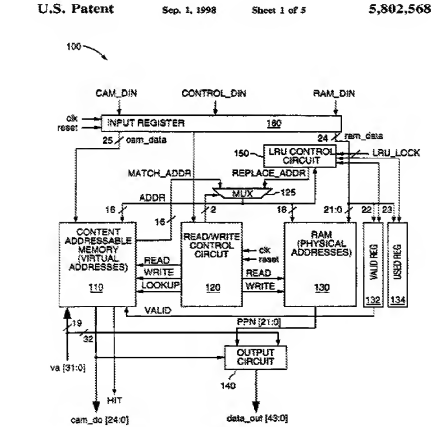

FIG. 1

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The primary reference teaches the input and output circuitry connected to the cache, however the Csoppenszky reference does not teach the caches as CAMRAM banks. Chai teaches the structuring a cache as a CAMRAM structure. It would have been obvious to one of ordinary skill in the caching art at the time the invention was made because CAMRAM structure is a specific integrated circuit chip for providing an interface between the CAM and RAM thereby improving the access between the two sections of the cache which would provide faster caching access.

As to claim 2, Csoppenszky teaches the present invention wherein cache input data selectively includes executable commands as stating many instruction units use instruction cache as well as data caches (e.g., see col. 1, lines 14-28).

As to claims 3, 11-12 and 20, Csoppenszky teaches the present invention wherein the cache buffer comprises a cache input buffer receiving cache input data as the input register (e.g., see Figure 1, element 160).

As to claims 4 and 13, Csoppenszky teaches the present invention wherein the cache buffer further comprises an output buffer where tag addresses in the tag memory are associated with the most recently accessed data which is sent to the output buffer as the addresses which are sent to the output buffer or circuit inherently receives the requested address or instructions/data which the processor of the system request in the last access request (e.g., see Figure 1).

As to claims 5-6 and 14-15, Csoppenszky teaches the present invention wherein the tag memory comprises a first content addressable memory (CAM) containing tags associated with data stored in the storage array (e.g., see Figure 1, element 110); and tags associated with the most recently accessed data (e.g., see col. 2, lines 10-56). The reference does not specifically

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teach a separate CAM for containing tags associated with the most recently accessed data, however, Chai teaches using multiple CAMs in conjunction with the RAM while selecting the portion of the RAM a CAM will be associated with. The RAM portion which has an associated CAM can be most recently accessed data as this data has heighten importance within the processing circuitry. It would have been obvious to one of ordinary skill in the cache art at the time the invention was made to associate a CAM tag with a RAM cache for purposes of access to the most recently accessed data because the most recently accessed data would be data in the cache buffer and by using a CAM for the TAG or TLB the access would be faster and more efficient as this is a common and fundamental reason for using a CAM for the addressing of the cache. (e.g., see the Summary of the Invention of the Chai reference). As to the second CAM be checked before the first CAM, this is more a labeling of the CAM as first and second as opposed to the functionality of the CAMs. If the second CAM is the CAM associated with the most recently accessed data portion of the cache, the checking of the second CAM prior to the first CAM would provide faster access to the data in the cache since the entire purpose of maintaining the most recently accessed data is established because this is data which is likely to be access again. This is a well established principle in the caching arts which is commonly referred to a rules of locality f or caching principles.

As to claim 8, Csoppenszky teaches the storage array comprises SRAM cells (e.g., see col. 6, lines 13-24).

As to claims 21 and 23, Csoppenszky teaches the stored data is marked as dirty as indicating whether or not the data is valid (e.g., see Figure 5).

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As to claims 25-29, Csoppenszky teaches the cache (and parts of the cache) is inherently checked for whether or not the requested data is present and if the data is not present, loading the data which is requested in the access command

6. Claims 7, 9, 16-17 and 24 read over the art of record.

RESPONSE TO APPLICANT'S REMARKS

7. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.

CONCLUSION

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Monday and Thursday from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

/Reba I. Elmore/
Primary Patent Examiner
Art Unit 2189

Monday, August 04, 2008

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